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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/774,818	02/09/2004	Mark G. Johnson	023-0025	9232

22120 7590 12/08/2005

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EXAMINER	
LE, THONG QUOC	
ART UNIT	**PAPER NUMBER**
2827	

DATE MAILED: 12/08/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/774,818	JOHNSON ET AL.	
	Examiner	Art Unit	
	Thong Q. Le	2827	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on *27 June 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-44* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *37-44* is/are allowed.

6)☒ Claim(s) *1,3,13,21 and 32* is/are rejected.

7)☒ Claim(s) *2,4-12,14-20,22-31 and 33-36* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *06/06/05,02/23/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Pre-amendment filed on 06/27/2005 has been entered.

2. Claims 1-44 are presented for examination.

Information Disclosure Statement

3. This office acknowledges receipt of the following items from the Applicant:

Information Disclosure Statement (IDS) filed on 02/23/2005.

Information Disclosure Statement (IDS) filed on 06/06/2005.

4. Information disclosed and list on PTO 1449 was considered.

Specification

5. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

7. Claims 1,3,13,21,32 are rejected under 35 U.S.C. 102(b) as being anticipated by Chappell et al. (U.S. Patent No. 4,845,669).

Regarding claims 1, Chappell et al. disclose an integrated circuit (Figure 5B) having two respective decode/selection circuits (52, 58, 56, 54) respectively located along opposite edges of a three-dimensional memory array (Column 1, lines 6-8, line 35) for selecting wordlines or bitlines (Figure 5B, WL, BL) which respectively exit the memory array along said opposite edges (Figure 5B, Column 3, lines 54-67, Column 4, lines 1-27).

Regarding claim 3, Chappell et al. disclose at least a portion of the two decode/selection circuits are disposed in a substrate upon which the memory array is formed (Figure 5B, 52, 56).

Regarding claim 13, Chappell et al. disclose an integrated circuit ((Figure 5B, 50) comprising a three-dimensional memory array (Column 1, lines 6-8) having at least two planes of memory cells formed above substrate (Figure 4) ; a first decode/selection circuit (Figure 5B, 52) having outputs associated with wordlines (Figure 5B, WL) or bitlines (figure 5B, BL) which exit on one edge of the memory array (Figure 5B) ; and a second decode/selection circuit (Figure 5B, 56) having outputs associated with wordlines or bitlines which exit on another edge opposite the one edge of the memory array (Figure 5B, Column 3, lines 54-67, Column 4, lines 1-27).

Regarding claim 21, Chappell et al. disclose first and second row selection circuit outputs which each connect to a respective wordline on each of at least two wordline layer (Figure 5B, WLI, WLII).

Regarding claim 32, Chappell et al. disclose the first and second decode/selection circuits are formed entirely in the substrate (Figure 5B).

Allowable Subject Matter

8. Claims 2,4-12,14-20,22-31,33-36 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claims 2,4-12,14-20,22-31,33-36 include allowable subject matter since the prior art made of record and considered pertinent to the applicant's disclosure does not teach or suggest the claimed limitations. Chappell et al. (U.S. Patent No. 4,845,669), and others, does not teach the claimed invention having an integrated circuit is structured as disclosed in each claims 2,4-12,14-20,22-31,33-36 .

9. Claims 37-44 are allowed.

Claims 37-44 include allowable subject matter since the prior art made of record and considered pertinent to the applicant's disclosure does not teach or suggest the claimed limitations. Chappell et al. (U.S. Patent No. 4,845,669), and others, does not teach the claimed invention having an integrated circuit comprising a first column selection circuit disposed at least partially beneath the memory array and having outputs along a north side of the memory array and associated with bitlines which exit the memory array to the north side.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thong Q. Le whose telephone number is 571-272-1783. The examiner can normally be reached on 8:00am-5:00pm M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Zarabian Amir can be reached on 571-272-1852. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Thong Q. Le
Primary Examiner
Art Unit 2827